Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0031	Serial No. 10/814,867
Information Disclosure Statement by Applicant	Applicant: Frederic Bernard et al.	
(Use several sheets if necessary)	Filed: March 30, 2004	Group: 2816

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
MT	A	2003/0206437	11/6/2003	Diorio et al.	365	185.03	
MT	B	2004/0004861	1/5/2004	Srinivas et al.	365	185.21	
MT	C	2004/0021166	2/5/2004	Hyde et al.	257	314	
MT	D	2004/0037127	2/26/2004	Lindhorst et al.	365	202	
MT	E	2004/0052113	3/18/2004	Diorio et al.	365	185.21	
MT	F	4,935,702	6/19/1990	Mead et al.	330	9	
MT	G	5,068,622	11/26/1991	Mead et al.	330	253	
MT	H	5,438,542	8/1/1995	Atsumi et al.	365	182	
MT	I	5,736,764	4/17/1998	Chang	257	318	
MT	J	5,777,926	7/7/1998	Trinh et al.	365	185.19	
MT	K	5,801,994	9/1/1998	Chang et al.	365	185.29	
MT	L	5,841,165	11/24/1998	Chang et al.	257	318	
MT	M	5,901,084	5/4/1999	Ohnakado	365	185.18	
MT	N	5,912,842	6/15/1999	Chang et al.	365	185.11	
MT	O	5,966,329	10/12/1999	Hsu et al.	365	185.18	
MT	P	5,982,669	11/6/1999	Kalnitsky et al.	365	185.28	
MT	Q	6,055,185	4/25/2000	Kalnitsky et al.	365	185.18	
MT	R	6,137,723	10/24/2000	Bergemont et al.	365	185.18	
MT	S	6,384,451	5/7/2002	Caywood	257	321	

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Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

MT	T	Invitation to Pay Additional Fees (Partial International Search), Application No. PCT/US 03/31792, date of mailing April 22, 2004.
MT	U	Declercq, et al., "Design and Optimization of High-Voltage CMOS Devices Compatible with a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4
MT	V	Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an, Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits, VOL. SC-11, No. 3, June 1976, pp. 374-378.
MT	W	Witters, et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits", IEEE Journal of Solid-State Circuits, VOL. 24, No. 5, October 1989, pp. 1372-1380.

Examiner	Date Considered
	10/13/05

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0031	Serial No. 10/814,867
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: March 30, 2004	Group: 2816

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date

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Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

MT	A	Carley, L. Richard, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1569-1575, December 1989.
MT	B	Partial International Search for International Application No. PCT/US03/31792, date mailed April 2, 2004.

Examiner	Date Considered
[signature]	10/13/05

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Information Disclosure Statement by Applicant	Applicant: Frederic Bernard et al.	
(Use several sheets if necessary)	Filed: March 30,2004 Group: ~~Unassigned~~ 2816	

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Init.		Document No.	Date	Name	Class	Subclass	Filing Date
MT	A	6,320,788	11/20/2001	Sansbury et al.	365	185.1	9/11/2000

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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner	Date Considered 10/13/05

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Information Disclosure Statement by Applicant	Applicant: Frederic Bernard et al.	
(Use several sheets if necessary)	Filed: ~~Herewith~~ 3/30/04	Group: ~~Unassigned~~ 2816

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Init.		Document No.	Date	Name	Class	Subclass	Filing Date
MT	A	5,761,121	6/2/1998	Chang	365	185.14	10/31/1996
MT	B	5,825,063	10/20/1998	Diorio et al.	257	316	7/26/1996
MT	C	5,875,126	2/23/1999	Minch et al.	365	185.01	9/26/1996
MT	D	5,898,613	4/27/1999	Diorio et al.	365	185.03	6/25/1997
MT	E	5,914,894	6/22/1999	Diorio et al.	365	185.03	6/1/1998
MT	F	5,986,927	11/16/1999	Minch et al.	365	185.01	11/10/1998
MT	G	5,990,512	11/23/1999	Diorio et al.	257	314	4/22/1997
MT	H	6,125,053	9/26/2000	Diorio et al.	365	185.03	11/30/1998
MT	I	6,144,581	11/7/2000	Diorio et al.	365	185.03	11/30/1998
MT	J	6,222,765	4/24/2001	Nojima	365	185.08	2/18/2000
MT	K	6,452,835	9/17/2002	Diorio et al.	365	185.03	10/27/2000
MT	L	6,477,103	11/5/2002	Nguyen et al.	365	225.7	9/21/2001
MT	M	6,661,278	12/9/2003	Gilliland	327	536	7/8/2002
MT	N	6,664,909	12/16/2003	Hyde et al.	341	144	8/13/2001

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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

MT	O	Raszka, Jaroslav, et al., "Embedded Flash Memory for Security Applications in a 0.13μm CMOS Logic Process", IEEE 2004 International Solid-State Circuits Conference, February 16, 2004, pp. 46-47.

Examiner	Date Considered 10/17/05

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Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0031	Serial No.: ~~Unassigned~~ 10/814867
Information Disclosure Statement by Applicant	Applicant: Frederic Bernard et al.	
(Use several sheets if necessary)	Filed: Herewith 3/30/04 Group: ~~Unassigned~~ 2816	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	P	~~2003/0206437~~	~~11/6/2003~~	~~Diorio et al.~~	~~365~~	~~185.03~~	~~7/9/2002~~
	Q	~~2004/0004861~~	~~1/8/2004~~	~~Srinivas et al.~~	~~365~~	~~185.21~~	~~7/5/2002~~
	R	~~2004/002/1166~~	~~2/5/2004~~	~~Hyde et al.~~	~~257~~	~~314~~	~~1/31/2003~~
	S	~~2004/0037127~~	~~2/26/2004~~	~~Lindhorst et al.~~	~~365~~	~~202~~	~~5/12/2003~~
	T	~~2004/0052113~~	~~3/18/2004~~	~~Diorio et al.~~	~~365~~	~~185.21~~	~~9/16/2002~~

Foreign Documents

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